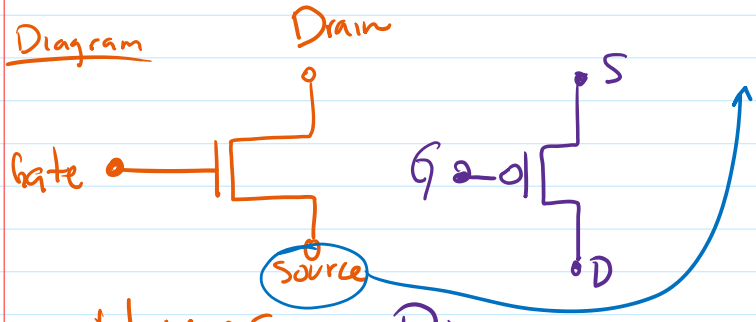
Transistors

Tuesday, June 23, 2020 11:45 AM

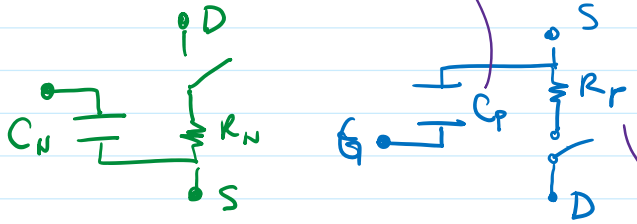
Diagram



Source: where the charge comes from

NMOS	PMOS
off: low voltage	off: high voltage
on: high voltage	on: low voltage

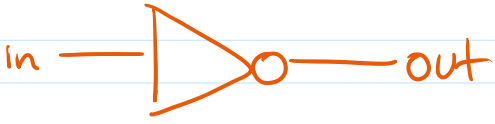
Simplified Model: gate capacitance

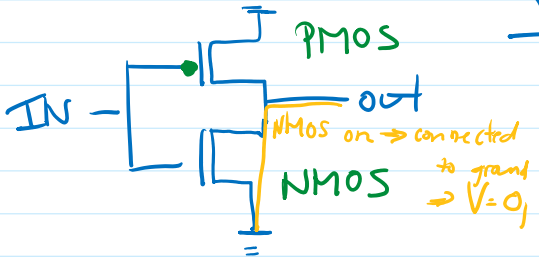


* V_{TH} = threshold voltage

	NMOS	PMOS
off:	$< V_{TH}$	$> V_{TH}$
on:	$> V_{TH}$	$< V_{TH}$

Inverter





V_{in}	NMOS	PMOS	V_{out}
V_{DD}	on	off	$V=0$, $P=0$
0	off	on	$V=V_{DD}$, $P=0$

Equations

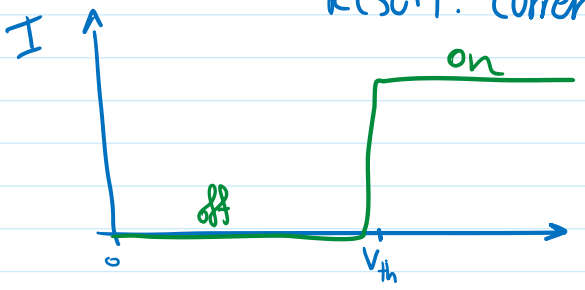
NMOS: $V_{GS} \geq V_{in}$ ← The voltage difference between S

Equations

NMOS: $V_{GS} \geq V_{in}$ ← The voltage difference between S and G must be positive.

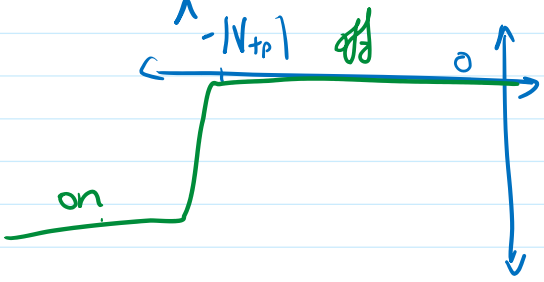
$V_{GS} = V_G - V_S$

Result: current flows from D to S



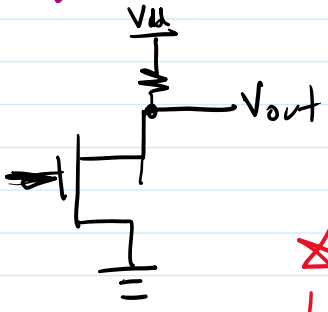
PMOS: $V_{SG} = V_S - V_G \geq 0$ ← S has higher voltage, D has lower voltage

Current flows from S to D



★ V_{th} always > 0

Single Transistor Inverter

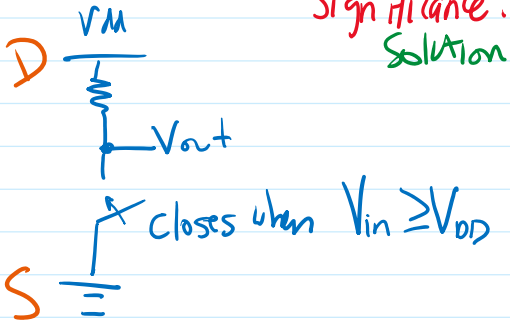


i) When $V_{in} = 0$, $V_{out} = V_{DD}$ (switch open)

ii) When $V_{in} = V_{DD}$, switch is on since $V_{GS} \geq V_{th}$
↳ Vout is connected directly to ground so $V_{out} = 0V$

★ iii) When open, $P = 0$ since $I = 0$
when closed, $P = \frac{V_{DD}^2}{R_1}$

Significance: transistors always consume power when activated
Solution: CMOS inverter



3 NAND Circuit

Let us consider a NAND logic gate. This circuit implements the boolean function $\overline{(A \cdot B)}$.

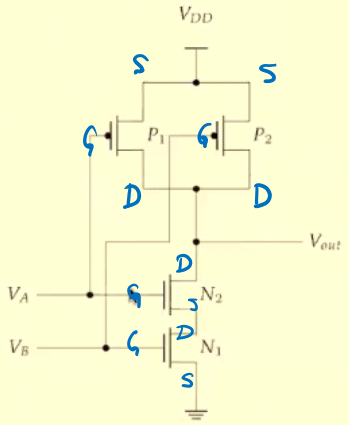


Figure 6: NAND

V_{tn} and V_{tp} are the threshold voltages for the NMOS and PMOS transistors, respectively. Assume that $V_{DD} > V_{tn}$ and $|V_{tp}| > 0$.

a) Label the gate, source, and drain nodes for the NMOS and PMOS transistors above.

V_A	V_B	N_1	N_2	P_1	P_2	V_{out}
V_{dd}	V_{dd}	on	on	off	off	0
0	V_{dd}	on	off	on	off	V_{dd}
V_{dd}	0	off	on	off	on	V_{dd}
0	0	off	off	on	on	V_{dd}